REMARKS

Applicants assert that the present invention is new, non-obvious and useful. Applicants respectfully request reconsideration of the above-identified application in view of the following remarks.

Status of Claims

Claims 1-3, 10-14, and 16-21 are pending in the application. Claims 4-9 and 15 were canceled without prejudice by previous amendment.

CLAIM REJECTIONS

35 U.S.C. § 103 Rejections

In the Office Action, the Examiner rejected claims 1-3, 10-12, and 16-20 under 35 U.S.C. §103(a) as being unpatentable over DiJaili (US 6,765,715) in view of Patel (US 2001/0015842). In addition, the Examiner rejected claims 13 and 14 under 35 U.S.C. §103(a) as being unpatentable over DiJaili in view of Patel and further in view of Jensen (US 4,632,518), and the Examiner also rejected claim 21 under 35 U.S.C. §103(a) as being unpatentable over DiJaili in view of Patel and further in view of Byun (US 6,804,047).

Applicants respectfully traverse these rejections in view of the following remarks.

With regards to independent claim 1, Applicants respectfully submit that neither DiJaili nor Patel, individually or in combination with other prior art references, including the references of Jensen and/or Byun, teach or suggest all elements of independent claim 1 or of the claims dependent thereon. Accordingly, Applicants respectfully assert that a prima facie case of obviousness has not been established and that the rejection under 35 U.S.C. §103 should be withdrawn.

Specifically, the references of DiJaili and Patel do not teach an all optical chopper including an optical splitter and an all optical AND logic gate "wherein said splitter is arranged to receive an optical input signal from said input terminal and to split the optical input signal into first and second optical signal components to exit at said first and second

output terminals, respectively, wherein said AND logic gate is arranged to receive said first and second optical signal components via said first and second inputs, and to produce at said output an optical output signal ... narrower than said optical input signal," as recited by Applicants' independent claim 1.

Initially, Applicants would like to point out that claim 1 is directed to a single-source optical chopper ("self-chopper"), which produces a chopped optical output signal in response to optical signal components split from the same optical input signal. This type of device, as described, for example, in Applicants' Figure 20a and paragraphs 244-251 of Applicants' specification, is different in purpose, structure and functionality from the devices described in the references cited by the Examiner; namely, an optical 2R/3R regenerator (DiJaili) and an optical bit rate converter (Patel). Therefore, in addition to the remarks below, Applicants respectfully submit that no combination of the cited references could result in, or show a motivation to create, an optical chopper as claimed by the present application.

In contrast to claim 1 of the present invention, DiJaili and Patel each describe an optical AND gate that operates on input signals received from two separate signal sources. The AND gate of DiJaili receives, at one input, an input optical signal and, at the second input, a clock signal of a variable oscillator (*see*, e.g., DiJaili, column 2 lines 29-32; column 3 lines 47-50; column 4, lines 20-30; and Figure 1). Similarly, the AND gate of Patel receives, at one input, an optical data bit pattern from an optical data source and, at the second input, an optical sampling bit stream from an optical sampler (*see*, e.g., Patel Figures 4, 5, and 8).

It is respectfully asserted that neither DiJaili nor Patel teach or suggest a single-source optical chopper, as required by Applicant's independent claim 1, and that, consequently, the cited combination of DiJaili and Patel certainly cannot teach at least this claimed feature of Applicants' invention. Accordingly, Applicants submit that a prima facie case of obviousness has not been established and, therefore, claim 1 is patentable over the prior art references of record.

Claims 2-3, 10-14, and 16-21 all depend from independent claim 1 and include all the elements of that claim, as well as additional distinguishing features. Thus, in addition to any independent basis for patentability, it is respectfully submitted that claims 2-3, 10-14, and 16-21 are likewise patentable at least by virtue of their dependency.

Furthermore, it is respectfully submitted that a person of ordinary skill in the art at the time the invention was made would not have been motivated to modify the AND gate of DiJaili with the splitter of Patel, as suggested by the Examiner. Although the Examiner points to paragraph 9 of Patel as providing motivation for combining the structure of a splitter with that of an AND gate "to improve the reliability and accuracy of the AND gate" (Office Action, page 4), Applicants note that paragraph 9 of Patel simply refers to "accurately rate converting" an ultra-high speed optical data bit stream to a lower rate optical data bit stream while maintaining the original sequence of bits. This accurate rate-conversion suggested by Patel has no bearing on the functionality of the optical regeneration device of DiJaili, or, for that matter, on the optical chopper of Applicants' invention.

In addition, even if the combination of Patel And DiJaili were proper (traversed by Applicants), the combination of DiJaili and Patel still would not result in the claimed structure of Applicants' invention as recited in independent claim 1, wherein the two outputs of an optical splitter are respectively associated with the two inputs of an all optical AND gate, and wherein one of the inputs of the AND gate includes an optical delay line.

As noted in Applicants' Remarks of April 20, 2006, the splitter of Patel is associated with only one input of the AND gate of Patel. Paragraphs 54-56 and Figure 3 of Patel describe a NOLM configured as an optical AND gate where an input port 86 functions as one of the logical inputs to the optical AND gate and an additional loop input port 98 functions as the second logical input to the optical AND gate. The structure of Patel functions as an optical AND gate because an output pulse 94 is only generated when both an optical input pulse 82 (introduced through input port 86 by way of a beam splitter 88) and an input optical pulse 100 (injected via the additional input port 98) are concurrently circulating in the optical fiber loop 84. Notwithstanding the Examiner's contention otherwise, it is clear from the description in Patel that the second input port 98 does not receive signals from splitter 88 in the way described by Applicants' claim 1. In the AND gate of Patel, the outputs of splitter 88 are the terminals that guide pulses 90 and 92. Unlike the structure described by Applicants' claim 1, input ports 86 and 98 of Patel are not associated with the output terminals of splitter 88.

In addition, Applicants also note that the time delay element of DiJaili (*see* DiJaili, Figure 11, and column 15 line 5 - column 16 line 6) is an internal element of the variable oscillator of DiJaili, rather than an optical delay line that is included in one of the optical AND gate inputs.

Conclusion

In view of the foregoing remarks, Applicants submit that the pending claims distinguish over the prior art of record and are in condition for allowance. Favorable consideration and passage to issue are therefore respectfully requested.

Applicants note that this Response is filed without a Request for Continued Examination in anticipation of an Advisory Action. The above notwithstanding, Applicants would appreciate an indication of the Examiner's position after reviewing this Response to allow Applicants the opportunity to file a Request for Continued Examination if deemed necessary.

The Examiner is invited to telephone the undersigned counsel at the number below to discuss any further issues yet to be resolved in connection with this application.

Please charge any fees associated with this paper to deposit account No. 50-3400.

Respectfully submitted,

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Dated: October 18, 2006

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